	Application No.	Applicant(s)
Notice of Allowability	09/801,913	TAKEUCHI ET AL.
	Examiner	Art Unit
	Jin-Cheng Wang	2628

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *3/9/2006*.

2. ☒ The allowed claim(s) is/are *1-27*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☒ All   b) ☐ Some*   c) ☐ None   of the:

      1. ☒ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

    * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

    (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached

      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.

    (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of ·
    Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)

2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)

3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____

4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

5. ☐ Notice of Informal Patent Application (PTO-152)

6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .

7. ☒ Examiner's Amendment/Comment

8. ☐ Examiner's Statement of Reasons for Allowance

9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and or

additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR

1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the

payment of the issue fee.

Claim 11:   (Currently Amended): A method of generating an overlay image signal composed

of an n number of superimposed image signals, n being an integer greater than 2, the method

comprising the steps of:

(a) digitally decoding a plurality of image signals by use of a plurality of respective

digital decoders;

(b) directly inputting outputs from each of the plurality of digital decoders to an image

selector;

(c) selecting from among the plurality of digitally decoded image signals, by use of the

image selector, one (1) reference image signal and (n-1) number of superimposing image signals;

(d) converting resolutions of the n number of selected image signals received directly

from the image selector, including the reference image signal and the (n-1) number of

superimposing image signals, into respective adjustable desired resolutions by use of a plurality

of resolution converters directly receiving respective outputs [of the] of the image selector, such

that any resolution converter can receive any output of the image selector; and

(e) superimposing the (n-1) number of converted superimposing image signals on the

converted reference signal, wherein an output of step (d) is output to step (e), and each of the

digital decoders can be connected to any of the resolution converters via the image selector.

Claim 20.   (Currently Amended): A method of generating an overlay image signal composed

of an n number of selected image signals, n being an integer greater than 2, the method

comprising the steps of:

(a) inputting a plurality of image signals directly from a plurality of respective digital

decoders to an image selector and selecting one (1) reference image signal and (n-1) number of

superimposing image signals from among the plurality of image signals;

(b) converting resolutions of the n number of selected image signals, including the

reference image signal and the (n-1) number of superimposing image signals, into

respective adjustable desired resolutions by use of a plurality of resolution converters

directly inputting respective outputs of the image selector, such that any resolution

converter can receive any output of the image selector; [and]

(c) first superimposing the (n-1) number of converted superimposing image signals on the

converted reference signal, the first superimposing receiving an output from a subset of a

plurality of steps (b); and

(d) second superimposing a directly received output form the first overlay processor and

another output of the plurality of steps (b),

wherein an output of step (b) is output to step [(e)] (d), and

each of the digital decoders can be connected to any of the resolution converters via the

image selector.

Reasons for Allowance

1.   The following is an examiner's statement of reasons for allowance of claims 1-5 in the

amendment of 6/23/2005: Nothing in the prior art anticipates or suggests, "a plurality of

resolution converters configured to _directly_ receive the selected image signals output from the

image selector" in an overlay image processing device for generating an overlay image signal

composed of an n number of selected image signals, n being an integer greater than 2, the

overlay image processing device comprising: a plurality of digital decoders configured to

digitally decode a plurality of image signals; an image selector configured to directly receive

outputs from each of the plurality of digital decoders and configured to select from among the

plurality of digitally decoded image signals one (1) reference image signal and (n-1) number of

superimposing image signals; a plurality of resolution converters configured to directly receive

the selected image signals output from the image selector, such that each resolution converter

can input any of the respective outputs, to convert resolutions of the n number of selected image

signals into respective adjustable desired resolutions, and to output the converted image signals

to an image synthesizer, wherein the image synthesizer is configured to superimpose the (n-1)

number of converted superimposing image signals on the converted one (1) reference signal, and

the image selector is configured to connect each of the digital decoders to any of the resolution

converters.

2.   The following is an examiner's statement of reasons for allowance of claims 6-10 and 24

in the amendment of 6/23/2005: Nothing in the prior art anticipates or suggests, "a plurality of

resolution converters configured to *directly* receive the selected image signals output from the

image selector" in an overlay image display device for displaying an overlay image composed of

an n number of selected images, n being an integer greater than 2, the overlay image display

device comprising: an overlay image processing device for generating an overlay image signal

composed of the n number of superimposed image signals; and an image display device for

displaying an image represented by the overlay image signal; wherein the overlay image

processing device includes: a plurality of digital decoders configured to digitally decode a

plurality of image signals; an image selector configured to directly receive outputs from each of

the plurality of digital decoders and configured to select from among the plurality of digitally

decoded image signals one (1) reference image signal and (n-1) number of superimposing image

signals; a plurality of resolution converters configured to directly receive the selected image

signals output from the image selector, such that each resolution converter can input any of the

respective outputs, to convert resolutions of the n number of selected image signals into

respective adjustable desired resolutions, and to output the converted signals to an image

synthesizer, wherein the image synthesizer is configured to superimpose the (n-1) number of

converted superimposing image signals on the converted one (1) reference signal, and the image

selector is configured to connect each of the digital decoders to any of the resolution converters.

3.   The following is an examiner's statement of reasons for allowance of claims 11-15 and

25 in the amendment of 6/23/2005: Nothing in the prior art anticipates or suggests, "each of the

digital decoders can be connected to *any* of the resolution converters via the image selector" in a

method of generating an overlay image signal composed of an n number of superimposed image signals, n being an integer greater than 2, the method comprising the steps of: (a) digitally decoding a plurality of image signals by use of a plurality of respective digital decoders; (b) directly inputting outputs from each of the plurality of digital decoders to an image selector; (c) selecting from among the plurality of digitally decoded image signals, by use of the image selector, one (1) reference image signal and (n-1) number of superimposing image signals; (d) converting resolutions of the n number of selected image signals received directly from the image selector, including the reference image signal and the (n-1) number of superimposing image signals, into respective adjustable desired resolutions by use of a plurality of resolution converters directly receiving respective outputs of the image selector, such that any resolution converter can receive any output of the image selector; and (e) superimposing the (n-1) number of converted superimposing image signals on the converted reference signal, wherein an output of step (d) is output to step (e), and each of the digital decoders can be connected to any of the resolution converters via the image selector.

4. The following is an examiner's statement of reasons for allowance of claims 16-19 and 26 in the amendment of 6/23/2005: Nothing in the prior art anticipates or suggests, "the image selector is configured to connect each of the digital decoders to _any_ of the resolution converters" in an overlay image processing device for generating an overlay image signal composed of an n number of selected image signals, n being an integer greater than 2, the overlay image processing device comprising: an image selector configured to select, from among a plurality of image signals received directly from a plurality of respectively digital decoders, one (1) reference image signal and (n-1) number of superimposing image signals; a plurality of resolution

converters configured to directly receive the selected image signals output from the image
selector, such that each resolution converter can input any of the respective outputs, to convert
resolutions of the n number of selected image signals to an image synthesizer, wherein the image
synthesizer is configured to superimpose the (n-1) number of converted superimposing image
signals on the converted one (1) reference signal, the image synthesizer includes first and second
overlay processors connected in series, the first overlay processor is configured to receive an
output from a subset of the plurality of resolution converters, and the second overlay processor is
configured to directly receive an output from the first overlay processor and another of the
plurality of resolution converters, and the image selector is configured to connect each of the
digital decoders to any of the resolution converters.

5.   The following is an examiner's statement of reasons for allowance of claims 20-23 and
27 in the amendment of 6/23/2005: Nothing in the prior art anticipates or suggests, "each of the
digital decoders can be connected to _any_ of the resolution converters via the image selector" in a
method of generating an overlay image signal composed of an n number of selected image
signals, n being an integer greater than 2, the method comprising the steps of: (a) inputting a
plurality of image signals directly from a plurality of respective digital decoders to an image
selector and selecting one (1) reference image signal and (n-1) number of superimposing image
signals from among the plurality of image signals; (b) converting resolutions of the n number of
selected image signals, including the reference image signal and the (n-1) number of
superimposing image signals, into respective adjustable desired resolutions by use of a plurality
of resolution converters directly inputting respective outputs of the image selector, such that any
resolution converter can receive any output of the image selector; (c) first superimposing the (n-

1) number of converted superimposing image signals on the converted reference signal, the first

superimposing receiving an output from a subset of a plurality of steps (b); and (d) second

superimposing a directly received output form the first overlay processor and another output of

the plurality of steps (b), wherein an output of step (b) is output to step wherein an output of step

(b) is output to step (d), and each of the digital decoders can be connected to any of the

resolution converters via the image selector.

6.   The cited reference, Odryna et al. U.S. Pat. No. 6,333,750 teaches a plurality of digital

decoders configured to digitally decode a plurality of image signals wherein each of the plurality

of digital decoder incorporated in each of the input cards, Input A, Input B, Input C of Figure 17.

Each of the input card as shown in Figure 21 has a digital decoder 182; see column 15-22.

        Odryna further teaches an image selector wherein a combination of control elements and

memories within the circuit blocks of Fig. 17 constitutes an image selector. For example, the

combination of the set of discrete elements such as the control block 111 shown in Fig. 18 within

the system card 110 of Fig. 17, the serial control bus 113 of Figs. 18 and 21, the control array

188 and the memories 186 shown in Fig. 21 within the Input A, or Input B, or Input C of Fig. 17

constitutes the image selector. This is because the control block 111 interconnected and bi-

directionally communicates with the serial control bus 113 and the control array 188 and

memories 186 interconnected and bi-directionally communicate with the serial control bus 113.

The plurality of circuit elements forms an integral control block that constitutes an image

selector. The integral control block is responsible for issuing the instructions for the overlay of

the image layers; see column 17. It also controls the control gate arrays within the other input

cards wherein each of the control gate arrays is programmed via the serial control buses 113; see

column 21. <u>Note that all the control gate arrays are programmed by the control block 111 of the</u>

<u>system card 110 via the serial control bus 113 to control the overlay of the base image with other</u>

<u>images.</u> <u>Odryna</u> thus teaches that the outputs of the decoder 182 are directly sent to the image

selector comprising the control array 188 of Fig. 21 and the control block 111 of Fig. 18.

<u>Odryna</u> teaches a plurality of resolution converters in which the **<u>scaler 184 of Figure 21</u>**

scales the input image and the common control gate array 120 within the system card 110

together with the pixel bus 114 defines how an overlay window is established (column 18, lines

1-15) and thus controls the display resolution. Therefore, the resolution of the input image is

controlled by the scaler 184 of each input card, the control gate array 120 of the system card 110

which controls the resolution of the overlay window associated with each input image through

the pixel bus 114. The discrete elements performs <u>a resolution conversion.</u> In column 20-21,

<u>Odryna</u> teaches another embodiments of the BVIDEO overlay card of Fig. 21 wherein the scaler

184 is utilized at the output of the buffer memory 186 and therefore the scaler 184 and the

control gate array 120 together with the pixel bus 114 as a whole directly receives image data

outputs from the buffer memory 186 which are controlled by the control gate array 188. Odryna

teaches a resolution converter within each of the input cards shown in Fig. 17 wherein the

resolution converter (scaler 184) directly receives image data outputs from <u>the image selector</u>

<u>comprising the buffer memory 186 and the control gate array 188 as well as the control block</u>

<u>111 and serial control bus 113</u>. Moreover, Odryna teaches a plurality of the resolution converters

because each of the plurality of the input cards, Input A, Input B, Input C of Fig. 17 has a scaler

184 together with the control gate array 120 and the pixel bus 114 which controls the resolution

of the window overlay from each of the input sources.

However, Odryna is not seen to disclose the claim limitation of "each of the digital

decoders can be connected to _any_ of the resolution converters via the image selector" set forth in

any of the independent claims 1, 6, 11, 16, and 20.

7.   Any comments considered necessary by applicant must be submitted no later than the

payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for

Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Jin-Cheng Wang whose telephone number is (571) 272-7665.

The examiner can normally be reached on 8:00 - 6:30 (Mon-Thu).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kee Tung can be reached on (571) 272-7794. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jcw

Kee M. Tung/
Primary Examiner